KY485LEEN

ESD-Enhanced, Fail-safe, Slew-Rate-limited RS-485/RS-422 Transceivers

General Description

The KY485LEEN +5V, half-duplex, ±20kV ESD-protected RS-485/RS-422-compatible transceivers feature one driver and one receiver.

The KY485LEEN include a hot-swap capability to eliminate false transitions on the bus during power-up or live insertion.

The KY485LEEN features reduced slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, allowing error-free transmission up to 1Mbps.

The KY485LEEN feature a 1/8-unit load receiver input impedance, allowing up to 256 transceivers on the bus. These devices are intended for half-duplex communications. All driver outputs are protected to ±20kV ESD using the Human Body Model and ±20kV ESD using the Air-Gap Discharge Model.

TheKY485LEEN is available in an 8-pin SO package.

The devices operate over the extended -40°C to +125°C temperature range.

Features

- +5V Operation
- Hot-Swappable for Telecom Applications
- Enhanced Slew-Rate Limiting Facilitates Error-Free Data Transmission
- Extended ESD Protection for RS-485 I/O Pins ±16kV
- High fanout driving 1/8Unit load , Allowing up to 256 Transceivers on the Bus.
- 8 Pin-SO Package

Applications

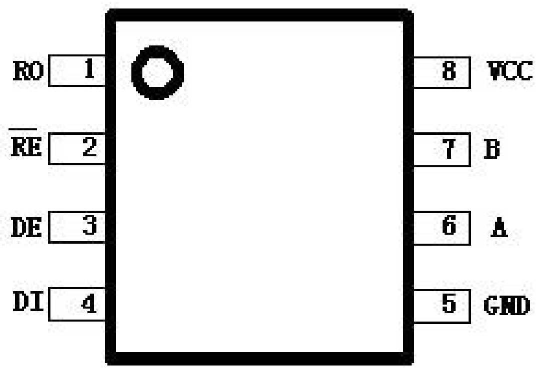
- Isolated RS-485 Interfaces
- Utility Meters
- Industrial Controls
- Industrial Motor Drives
- Automated HVAC Systems

Absolute Maximum Ratins (All voltages referenced to GND.)

Supply Voltage VCC...+6V
DE, RE-, DI...-0.3V to +6
A, B... -8V to +13V
Short-Circuit Duration (RO, A, B) to GND ....Continuous
Continuous Power Dissipation (TA = +70°C)
8-Pin SO (derate 5.9mW/°C above +70°C).................471mW
Operating Temperature Range ....-40°C to +125°C
Junction Temperature..+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

KY485LEEN



Package SOIC8

Package Information

DC Electrical Characteristics

(VCC = +5V ± 5%, TA = TMIN to TMAX, unless otherwise noted. Typical values are at VCC = +5V and TA = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DRIVER							
Differential Driver Output (no load)	V_{OD1}	Figure1				5	V
Differential Driver Output	V_{OD2}	Figure1,R = 50Ω (RS-422)		2.0			V
		Figure1,R = 27Ω (RS-485)		1.5			
Change in Magnitude of Differential Output Voltage (Note 2)	ΔV_{OD}	Figure1,R =50Ωor R= 27Ω				0.2	V
Driver Common-Mode Output Voltage	V_{OC}	Figure1,R=50Ωor R = 27Ω				3	V
Change In Magnitude of Common-Mode Voltage (Note 2)	ΔV_{OC}	Figure1,R=50Ωor R = 27Ω				0.2	V
Input High Voltage	V_{IH1}	DE , DI , $\overline{RE}$		2.0			V
Input Low Voltage	V_{IL1}	DE, DI, $\overline{RE}$				0.8	V
DI Input Hysteresis	V_{HYS}	KY485LEEN		100			mV
Input Current	I_{IN1}	DE, DI, $\overline{RE}$				±2	μA
Input Current (A and B)	I_{IN4}	DE = GND, V_{CC}=GND or 5.25V	V_{IN}=12V			125	μA
			V_{IN} = -7V	-75			
Driver Short-Circuit Output Current (Note 3)	V_{OD1}	-7V ≤ V_{OUT} ≤ V_{CC}		-250			mA
		0V ≤ V_{OUT} ≤ 12V				250	mA
		0V ≤ V_{OUT} ≤ V_{CC}		±25			mA
RECEIVER							
Receiver Differential Threshold Voltage	V_{TH}	-7V ≤ V_{CM} ≤ +12V		-200	-125	-50	mV
Receiver Input Hysteresis	ΔV_{TH}			25			mV
Receiver Output High Voltage	V_{OH}	I_O = 4mA, V_{ID} = -200mV;		Vcc-1.5			V
Receiver Output Low Voltage	V_{OL}	I_O = -4mA, V_{ID} = -50mV				0.4	V
Three-State Output Current at Receiver	I_{OZR}	0.4V ≤ V_O ≤ 2.4V				±1	μA
Receiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ +12V		96			kΩ
Receiver Output Short-Circuit Current	I_{OSR}	0V ≤ V_{RO} ≤ V_{CC}		±7		±95	mA
SUPPLY CURRENT							
Supply Current	I_{CC}	No load, RE- =DI=GND or VCC	DE = VCC		530	900	μA
			DE = GND		500	600	
Supply Current in Shutdown Mode	I_{SHDN}	DE = GND, V_{RE-} = V_{CC}			2.5	10	μA
ESD Protection							
ESD Protection(A,B)		Air Gap Discharge IEC 61000-4-2			±16		KV
		Human Body Model			±8		
ESD Protection(all other pins)		Human Body Model			±5		KV

Note 1: All currents into the device are positive; all currents out of the device are negative. All voltages are referred to device

ground unless otherwise noted.

Note 2: ΔVOD and ΔVOC are the changes in VOD and VOC, respectively, when the DI input changes state.

Note 3: Maximum current level applies to peak current just prior to fold-back-current limiting; minimum current level applies during current limiting.

Switching Characteristics

(VCC = +5V ±5%, TA = TMIN to TMAX, unless otherwise noted. Typical values are at VCC = +5V and TA = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Input to Output	t_{DPLH}	Figures3 and 5, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	250 1000	720		ns
	t_{DPHL}		250 1000	720		
Driver Output Skew ∣ t_{DPLH} - t_{DPHL} ∣	t_{DSKEW}	Figures 3 and 5, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	±100	-3		ns
Driver Rise or Fall Time	t_{DR}, t_{DF}	Figures 3 and 5, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	200	530	750	ns
Maximum Data Rate	f_{MAX}			1000	2000	kbps
Driver Enable to Output High	t_{DZH}	Figures4 and 6, C_L = 100pF, S2 closed			2500	ns
Driver Enable to Output Low	t_{DZL}	Figures4 and 6,C_L= 100pF, S1 closed			2500	ns
Driver Disable Time from Low	t_{DLZ}	Figures 4 and 6, C_L = 15pF, S1 closed			100	ns
Driver Disable Time from High	t_{DHZ}	Figures 4 and 6, C_L = 15pF, S2 closed			100	ns
Receiver Input to Output	t_{RPLH}, t_{RPHL}	Figures 7 and 9; ∣ V_{ID} ∣ ≥ 2.0V;rise and fall time of V_{ID} ≤ 15ns		200	250	ns
∣ t_{RPLH} - t_{RPHL} ∣ Differential Receiver Skew	t_{RSKD}	Figures 7 and 9; ∣ V_{ID} ∣ ≥ 2.0V;rise and fall time of V_{ID} ≤ 15ns		3	±30	ns
Receiver Enable to Output Low	t_{RZL}	Figures 2 and 8, C_L = 100pF, S1 closed		20	50	ns
Receiver Enable to Output High	t_{RZH}	Figures 2 and 8, C_L = 100pF, S2 closed		20	50	ns
Receiver Disable Time from Low	t_{RLZ}	Figures 2 and 8 , C_L = 100pF, S1 closed		20	50	ns
Receiver Disable Time from High	t_{RHZ}	Figures 2 and 8, C_L = 100pF, S2 closed		20	50	ns
Time to Shutdown	t_{SHDN}	(Note 4)	50	200	600	ns
Driver Enable from Shutdown to Output High	$t_{DZH(SHDN)}$	Figures 4 and 6, C_L = 15pF, S2 closed			4500	ns
Driver Enable from Shutdown to Output Low	$t_{DZL(SHDN)}$	Figures 4 and 6, C_L = 15pF, S1 closed			4500	ns
Receiver Enable from Shutdown to Output High	$t_{RZH(SHDN)}$	Figures 2 and 8, C_L = 100pF, S2 closed			3500	ns
Receiver Enable from Shutdown to Output Low	$t_{RZL(SHDN)}$	Figures 2 and 8, C_L = 100pF, S1 closed			3500	ns

Note 4: The device is put into shutdown by bringing $\overline{RE}$ high and DE low. If the enable inputs are in this state for less than 50ns, the device is guaranteed not to enter shutdown. If the enable inputs are in this state for at least 600ns, the device is guaranteed to have entered shutdown.

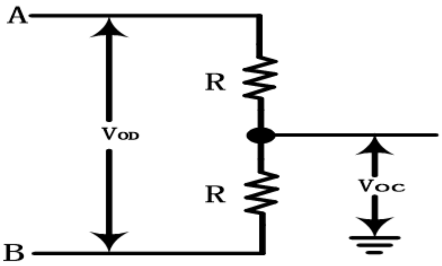


Figure 1 Driver DC Test Load

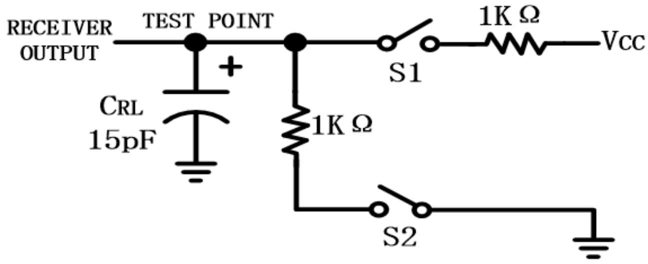


Figure 2 Receiver Enable/Disable Timing Test Load

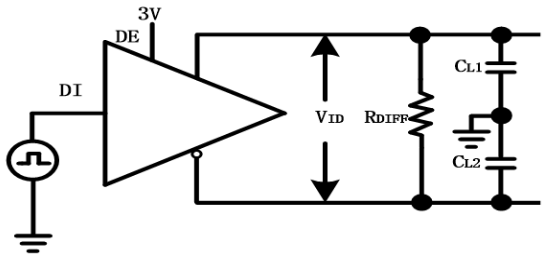


Figure 3 Driver Timing Test Circuit

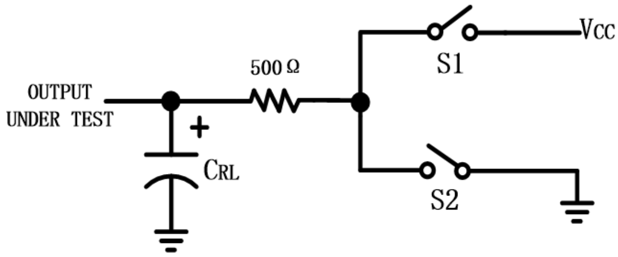


Figure 4 Driver Enable/Disable Timing Test Load

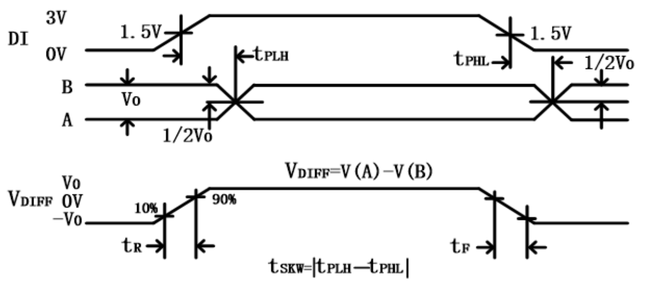


Figure 5 Driver Propagation Delays

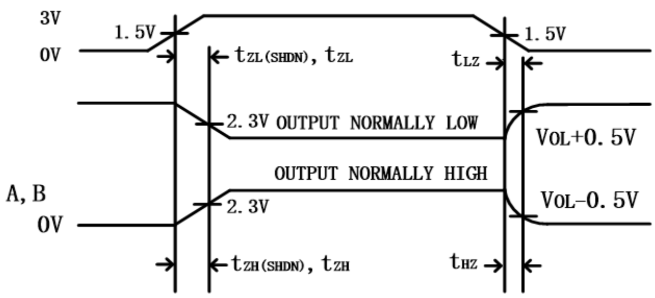


Figure 6 Driver Enable and Disable Times

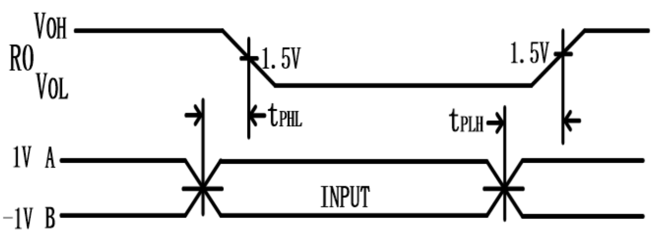


Figure 7 Receiver Propagation Delays

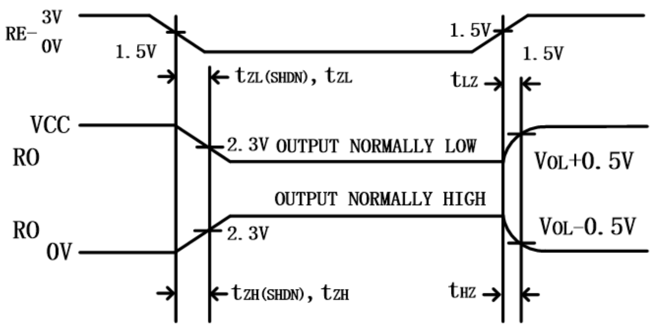


Figure 8 Receiver Enable and Disable Times

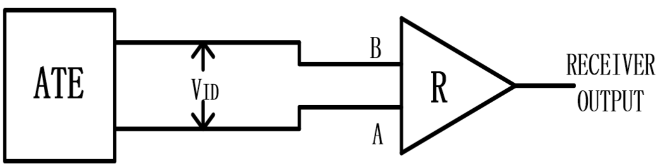


Figure 9 Receiver Propagation Delay Test Circuit

Pin Description

PIN	NAME	FUNCTION
1	RO	Receiver Output. When RE is low and if A - B ≥ -50mV, RO will be high; if A - B ≤ -200mV, RO will be low.
2	$\overline{RE}$	Receiver Output Enable. Drive RE low to enable RO; RO is high impedance when RE is high. Drive RE high and DE low to enter low-power shutdown mode. RE is a hot-swap input (see the *Hot-Swap Capability* section for more details).
3	DE	Driver Output Enable. Drive DE high to enable driver outputs. These outputs are high impedance when DE is low. Drive RE high and DE low to enter low-power shutdown mode. DE is a hot-swap input (see the *Hot-Swap Capability* section for more details).
4	DI	Driver Input. With DE high, a low on DI forces non-inverting output low and inverting output high. Similarly, a high on DI forces non-inverting output high and inverting output low.
5	GND	Ground
6	A	Non-inverting Receiver Input and Non-inverting Driver Output
7	B	Inverting Receiver Input and Inverting Driver Output
8	Vcc	Positive Supply, V_{CC} = +5V ±5%. Bypass V_{CC} to GND with a 0.1μF capacitor.

Function Table

TRANSMITTING				
INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	B/Z	A/Y
X	1	1	0	1
X	1	0	1	0
0	0	X	High-Z	High-Z
1	0	X	Shutdown	

RECEIVING			
INPUTS			OUTPUTS
$\overline{RE}$	DE	A-B	RO
0	X	≥ -0.05V	1
0	X	≤ -0.2V	0
0	X	Open/shorted	1
1	1	X	High-Z
1	0	X	Shutdown

Applications Information

256 Transceivers on the Bus

The standard RS-485 receiver input impedance is 12kΩ (one-unit load), and the standard driver can drive up to 32 unit loads. The KY485LEEN family of transceivers have a 1/8-unit-load receiver input impedance (96kΩ), allowing up to 256 transceivers to be connected in parallel on one communication line. Any combination of these devices and/or other RS-485 transceivers with a total of 32 unit loads or less can be connected to the line.

Low-Power Shutdown Mode

Low-power shutdown mode is initiated by bringing both RE- high and DE low. In shutdown, the devices typically draw only 2uA of supply current.
RE- and DE may be driven simultaneously; the parts are guaranteed not to enter shutdown if
RE is high and DE is low for less than 50ns. If the inputs are in this state for at least 600ns, the parts are guaranteed to enter shutdown.

Reduced EMI and Reflections

KY485LEEN is slew-rate limited, minimizing EMI and reducing reflections caused by improperly terminated cables.

Driver Output Protection

Two mechanisms prevent excessive output current and power dissipation caused by faults or by bus contention. The first, a fold-back current limit on the output stage, provides immediate protection against short circuits over the whole common-mode voltage range (see Typical Operating Characteristics). The second, a thermal shutdown circuit, forces the driver outputs into a high-impedance state if the die temperature becomes excessive.

Fail-Safe

The KY485LEEN guarantees a logic-high receiver output when the receiver inputs are shorted or open, or when they are connected to a terminated transmission line with all drivers disabled. This is done by setting the receiver threshold between -50mV and -200mV. If the differential receiver input voltage (A-B) is greater than or equal to -50mV, RO is logic high. If A-B is less than or equal to -200mV, RO is logic low. In the case of a terminated bus with all transmitters disabled, the receiver's differential input voltage is pulled to 0V by the termination. With the receiver thresholds of KY485LEEN, this results in a logic high with a 50mV minimum noise margin. Unlike previous fail-safe devices, the -50mV to -200mV threshold complies with the ±200mV EIA/TIA-485 standard.

Hot-Swap Capability

When circuit boards are inserted into a hot or powered back plane, differential disturbances to the data bus can lead to data errors. Upon initial circuit-board insertion, the data communication processor undergoes its own power-up sequence. During this period, the processor's logic-output drivers are high impedance and are unable to drive the DI and RE- inputs of these devices to a defined logic level. Leakage currents up to ±10μA from the high-impedance state of the processor's logic drivers could cause standard CMOS enable inputs of a transceiver to drift to an incorrect logic level.
Additionally, parasitic circuit-board capacitance could cause coupling of VCC or GND to the enable inputs. Without the hot-swap capability, these factors could improperly enable the transceiver's driver.
To overcome both these problems, When VCC rises, an internal power-up signal Turn from low to high and keeps about 20uS then turns to low. During the 20uS high stage, this signal controls the internal logic to force to disable the driver and enable the receiver regardless the state of the DE and RE-.

ESD Protection

As with all KEYSEMI devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handing and assembly. The driver outputs and receiver inputs of KY485LEEN have extra protection against static electricity. KEYSEMI's engineers have developed state-of-the-art structures to protect these pins against ESD of ±20kV without damage. The ESD structures withstand high ESD in all states: normal operation shutdown, and powered down. After an ESD event the KY485LEEN keep working without latch-up or damage.
ESD protection can be tested in various ways. The transmitter outputs and receiver inputs of the KY485LEEN are characterized for protection to the following limits:

- ±20kV using the Human Body Model
- ±20kV using the Air Gap Discharge Method specified in IEC61000-4-2

ESD Test Conditions

ESD performance depends on a variety of

conditions. Contact GIC for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 10a shows the Human Body Model, and Figure10b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

IEC 61000-4-2

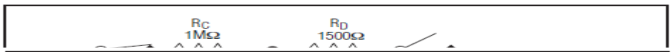
The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The KY485LEEN help you design equipment to meet IEC 61000-4-2 without the need for additional ESD-protection components.
The major difference between tests done using the
Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2 because series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the Human Body Model. Figure 10c shows the IEC 61000-4-2 model, and Figure 10d shows the current waveform for IEC61000-4-2 ESD Contact Discharge test.

Machine Model

The machine model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. The objective is to emulate the stress caused when I/O pins are contacted by handling equipment during test and assembly. Of course, all pins require this protection, not just RS-485 inputs and outputs. The Air-Gap test involves approaching the device with a charged probe. The Contact-Discharge method connects the probe to the device before the probe is energized.

Typical Applications

The KY485LEEN transceiver is designed for bidirectional data communications on multipoint bus transmission lines. Figure 11 shows typical network applications circuits.
To minimize reflections, the line should be terminated at both ends in its characteristic impedance, and stub lengths off the main line should be kept as short as possible.



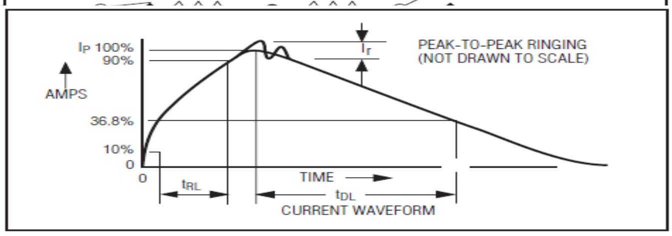
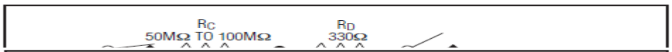


Figure 10a Human Body ESD Test Model

Figure 10b Human Body Current Waveform



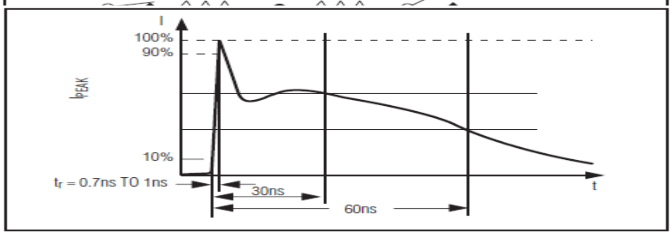


Figure 10c IEC 61000-4-2 ESD Test Model

Figure 10d IEC 61000-4-2 ESD Current Waveform

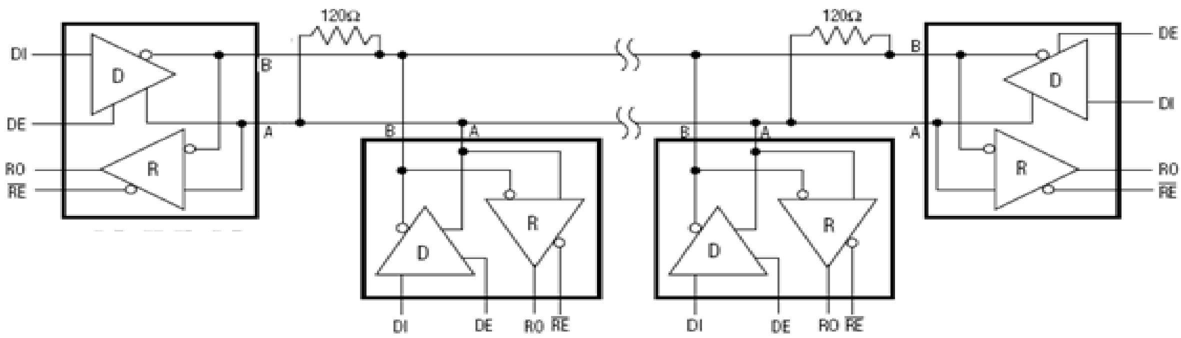
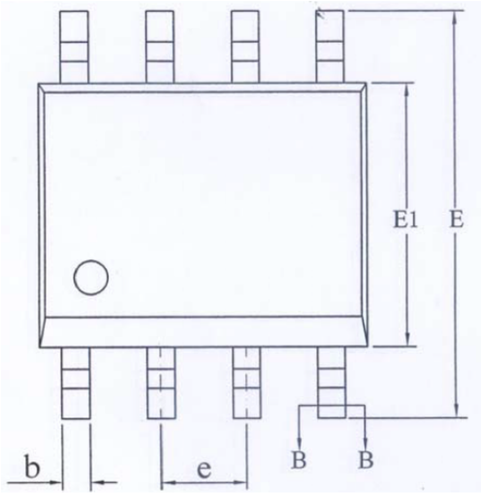


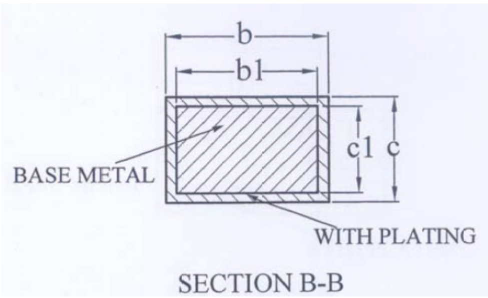
Figure 11 Typical Half-Duplex RS-485 Network

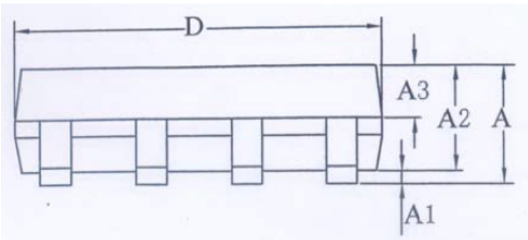
KY485LEEN

Outline Dimension

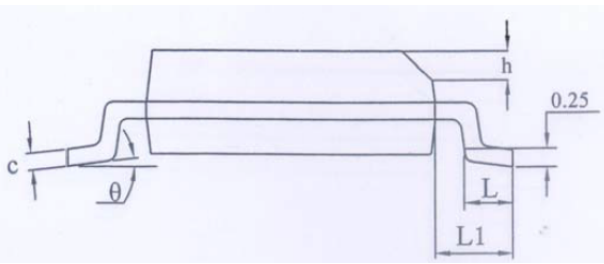


TOP VIEW





FRONT VIEW



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.48
b1	0.38	0.41	0.43
c	0.21	—	0.26
c1	0.19	0.20	0.21
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05BSC		
θ	0	—	8°
LF载体尺寸 (mil)	80*80	90*90	95*130